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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/619,477	07/19/2000	Shunpei Yamazaki	0756-2178	1881

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ERIC ROBINSON
PMB 955
21010 SOUTHBANK ST.
POTOMAC FALLS, VA 20165

EXAMINER	
ROSE, KIESHA L	
ART UNIT	PAPER NUMBER
2822	

SHORTENED STATUTORY PERIOD OF RESPONSE	MAIL DATE	DELIVERY MODE
3 MONTHS	04/04/2007	PAPER

Please find below and/or attached an Office communication concerning this application or proceeding.

If NO period for reply is specified above, the maximum statutory period will apply and will expire 6 MONTHS from the mailing date of this communication.

Office Action Summary	Application No.	Applicant(s)	
	09/619,477	YAMAZAKI, SHUNPEI	
	Examiner	Art Unit	
	Kiesha L. Rose	2822	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *09 January 2007*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☐ Claim(s) _____ is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *31,32,35-43,46-53,55,56,59-61,63,65-67 and 69* is/are rejected.

7)☒ Claim(s) *62,64,68 and 70* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date *1/9/07*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

This Office Action is in response to the RCE filed 15 August 2006.

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claims 31,32,35-37,39,42,55,59,60,61 and 63 are rejected under 35 U.S.C. 103(a) as being unpatentable over Applicant's Prior Art (Fig. 30) in view of Ono et al. (U.S. Patent 5,668,379).

In re claim 31, Applicant's Prior Art (Fig. 30) discloses a semiconductor device that contains a first substrate (1), a thin film transistor over first substrate (Page 2, lines 11-13, both transistor, wiring and connecting wire are formed on the same substrate), a second substrate (5) opposing first substrate, a wiring (6) provided with second substrate, a connecting wiring (3) for electrically connecting wiring of the second substrate to thin film transistor over first substrate (Page 2, lines 19-21, the connecting wire is formed to supply power and input signals to the driver circuit, which is the thin film transistor), wherein connecting wiring comprises a metallic film (3a) over first substrate and a transparent conductive film (3b) over metallic film, an insulating film (2) over the substrate, an anisotropic conductive film (7) over the insulating film and the

connecting wiring, wherein the wiring of the second substrate is connected to a portion of the connecting wiring and wherein both side surfaces of the portion of the connecting wiring are in contact with the insulating film. (Since the connecting wiring contains two layers as seen in Fig. 30, layer 3a has both side surfaces (the left and right side of the metallic layer 3a) that is connected to the insulating layer.) Applicant's Prior Art discloses all the limitations except for the metallic film to have a tapered shape. Whereas Ono discloses a thin film transistor (Fig. 17) that contains a metallic film with a taper shape. Ono discloses the metallic film (d1) to have a tapered shape to reduce breakage and gate/drain short circuit can be suppressed. (Column 4, lines 65-67 and Column 5, lines 1-2) Therefore it would have been obvious to one having ordinary skill in the art at the time the invention was made to modify the device of Applicant's Prior Art (Fig. 30) by incorporating the metallic film to have a tapered shape to reduce breakage and gate/drain short circuit can be suppressed as taught by Ono.

In re claim 32, Ono discloses the insulating film (PSV1) comprises the same material (silicon nitride) as that contained in an insulating film (GI) between a gate wiring and a source wiring of the thin film. (Fig. 3, Column 9, lines 10-11 and Column 12, lines 14-15)

In re claim 35, Ono discloses the metallic film (d1) to have a thickness between 100 nm and 1 micron. (Column 9, lines 35-38)

In re claim 36, Applicant's Prior Art discloses the metallic film comprises aluminum. (Page 3, lines 9-10)

In re claim 37, Ono discloses the metallic film to comprise tungsten (W). (Column 9, lines 41-43)

In re claim 39, Ono discloses the transparent conductive film (d2) to have a thickness between 50 nm and 0.5 microns. (Column 10, lines 33-35)

In re claim 42, Applicant's Prior Art discloses the semiconductor device is one of a liquid crystal display device and EL display device. (Page 1, lines 14-15)

In re claim 55, Ono discloses the connecting wiring the same materials as the source wiring and the drain wiring of the thin film transistor. (Figs. 5 and 7 (Both the connecting wiring and source/drain wiring are formed of metallic film (d1) and transparent conductive film (d2))

In re claim 59, Applicant's Prior art discloses the anisotropic conductive film covers the portion of the connecting wiring.

In re claim 60, Applicant's Prior art discloses the thin film transistor is a top gate thin film transistor. (Page 2, lines 13-16, since the thin film transistor is a CMOS then it would be a top gate transistor)

In re claim 61, Applicant's Prior Art discloses the anisotropic conductive film comprises a conductive grain (8) dispersed to an adhesive (9). (Fig. 30)

In re claim 63, Applicant's Prior Art discloses the thin film transistor is formed in a driver circuit. (Page 2, lines 19-21)

Claim 38 is rejected under 35 U.S.C. 103(a) as being unpatentable over Applicant's Prior Art (Fig. 30) and Ono as applied to claim 31 above, and further in view of Ukita (U.S. Patent 5,821,159).

In re claim 38, Applicant's Prior Art and Ono disclose all the limitations except for the metallic film to comprise tungsten and a lamination film of tungsten nitride. Whereas Ukita discloses a thin film transistor (Fig. 6) that contains a metallic film (45) made of tungsten with a tungsten nitride layer (46) formed thereon. Tungsten nitride is formed on the tungsten layer to suppress low resistive metal from being dissolved and to prevent corrosion of the metal by the etchant. (Column 4, lines 44-50) Therefore it would have been obvious to one having ordinary skill in the art at the time the invention was made to modify the devices of Applicant's Prior Art and Ono by incorporating tungsten nitride on the tungsten layer to suppress low resistive metal from being dissolved and to prevent corrosion of the metal by the etchant as taught by Ukita.

Claims 40-41 are rejected under 35 U.S.C. 103(a) as being unpatentable over Applicant's Prior Art (Fig. 30) and Ono as applied to claim 31 above, and further in view of Utsumi et al. (U.S. Patent 6,215,077)

In re claims 40-41, Applicant's Prior Art and Ono disclose all the limitations except for the transparent conductive film to comprise zinc oxide and indium oxide. Whereas Utsumi discloses a thin film device (Fig. 1) that contains a transparent conductive film (3b) that comprises zinc oxide and indium oxide. (Column 4, lines 56-58) The transparent conductive film is formed of zinc oxide and indium oxide to prevent

hillocks from being formed on first and second conductors. (Column 3, lines 64-67 and Column 4, lines 1-3) Therefore it would have been obvious to one having ordinary skill in the art at the time the invention was made to modify the devices of Applicant's Prior Art and Ono by incorporating the transparent conductive film to comprise zinc oxide and indium oxide to prevent hillocks from being formed on first and second conductors as taught by Utsumi.

Claims 43,46-48,50,53,56,65,66,67 and 69 are rejected under 35 U.S.C. 103(a) as being unpatentable over Applicant's Prior Art (Fig. 30) in view of Ono and further in view of Hioki (JP 8-234212).

In re claim 43, Applicant's Prior Art (Fig. 30) discloses a semiconductor device that contains a first substrate (1), a thin film transistor over first substrate (Page 2, lines 11-13, both transistor, wiring and connecting wire are formed on the same substrate), a second substrate (5) opposing first substrate, a wiring (6) provided with second substrate, a connecting wiring (3) for electrically connecting wiring of the second substrate to thin film transistor over first substrate (Page 2, lines 19-21, the connecting wire is formed to supply power and input signals to the driver circuit, which is the thin film transistor), wherein connecting wiring comprises a metallic film (3a) over first substrate and a transparent conductive film (3b) over metallic film, an insulating film (2) over the substrate, an anisotropic conductive film (7) over the insulating film and the connecting wiring, wherein the wiring of the second substrate is connected to a portion of the connecting wiring and wherein both side surfaces of the portion of the connecting

wiring are in contact with the insulating film. (Since the connecting wiring contains two layers as seen in Fig. 30, layer 3a has both side surfaces (the left and right side of the metallic layer 3a) that is connected to the insulating layer.) Applicant's Prior Art discloses all the limitations except for the metallic film to have a tapered shape. Whereas Ono discloses a thin film transistor (Fig. 17) that contains a metallic film with a taper shape. Ono discloses the metallic film (d1) to have a tapered shape to reduce breakage and gate/drain short circuit can be suppressed. (Column 4, lines 65-67 and Column 5, lines 1-2) Therefore it would have been obvious to one having ordinary skill in the art at the time the invention was made to modify the device of Applicant's Prior Art (Fig. 30) by incorporating the metallic film to have a tapered shape to reduce breakage and gate/drain short circuit can be suppressed as taught by Ono. Applicant's Prior Art and Ono disclose all the limitations except for a column-shape spacer. Whereas Hioki discloses a liquid crystal display (Fig. 1) that contains a column-shape spacer (24) over thin film transistor (18/20) between first substrate (14) and second substrate (26). The column-shape spacer is formed for intra-surface uniformity. (Constitution) Therefore it would have been obvious to one having ordinary skill in the art at the time the invention was made to modify the devices of Applicant's Prior Art (Fig. 30) and Ono by incorporating a column-shape spacer for intra-surface uniformity as taught by Hioki.

In re claim 46, Ono discloses the metallic film (d1) to have a thickness between 100nm and 1 micron. (Column 9, lines 35-38)

In re claim 47, Applicant's Prior Art discloses the metallic film comprises aluminum. (Page 3, lines 9-10)

In re claim 48, Ono discloses the metallic film to comprise tungsten (W). (Column 9, lines 41-43)

In re claim 50, Ono discloses the transparent conductive film (d2) to have a thickness between 50 nm and 0.5 microns. (Column 10, lines 33-35)

In re claim 53, Applicant's Prior Art discloses the semiconductor device is one of a liquid crystal display device and EL display device. (Page 1, lines 14-15)

In re claim 56, Ono discloses the connecting wiring the same materials as the source wiring and the drain wiring of the thin film transistor. (Figs. 5 and 7 (Both the connecting wiring and source/drain wiring are formed of metallic film (d1) and transparent conductive film (d2))

In re claim 65, Applicant's Prior art discloses the anisotropic conductive film covers the portion of the connecting wiring.

In re claim 66, Applicant's Prior art discloses the thin film transistor is a top gate thin film transistor. (Page 2, lines 13-16, since the thin film transistor is a CMOS then it would be a top gate transistor)

In re claim 67, Applicant's Prior Art discloses the anisotropic conductive film comprises a conductive grain (8) dispersed to an adhesive (9). (Fig. 30)

In re claim 69, Applicant's Prior Art discloses the thin film transistor is formed in a driver circuit. (Page 2, lines 19-21)

Claim 49 is rejected under 35 U.S.C. 103(a) as being unpatentable over Applicant's Prior Art (Fig. 30), Ono and Hioki as applied to claim 43 above, and further in view of Ukita.

In re claim 49, Applicant's Prior Art, Ono and Hioki disclose all the limitations except for the metallic film to comprise tungsten and a lamination film of tungsten nitride. Whereas Ukita discloses a thin film transistor (Fig. 6) that contains a metallic film (45) made of tungsten with a tungsten nitride layer (46) formed thereon. Tungsten nitride is formed on the tungsten layer to suppress low resistive metal from being dissolved and to prevent corrosion of the metal by the etchant. (Column 4, lines 44-50) Therefore it would have been obvious to one having ordinary skill in the art at the time the invention was made to modify the devices of Applicant's Prior Art, Ono and Hioki by incorporating tungsten nitride on the tungsten layer to suppress low resistive metal from being dissolved and to prevent corrosion of the metal by the etchant as taught by Ukita.

Claims 51-52 are rejected under 35 U.S.C. 103(a) as being unpatentable over Applicant's Prior Art (Fig. 30), Ono and Hioki as applied to claim 43 above, and further in view of Utsumi et al.

In re claims 51-52, Applicant's Prior Art, Ono and Hioki disclose all the limitations except for the transparent conductive film to comprise zinc oxide and indium oxide. Whereas Utsumi discloses a thin film device (Fig. 1) that contains a transparent conductive film (3b) that comprises zinc oxide and indium oxide. (Column 4, lines 56-58) The transparent conductive film is formed of zinc oxide and indium oxide to prevent

hillocks from being formed on first and second conductors. (Column 3, lines 64-67 and Column 4, lines 1-3) Therefore it would have been obvious to one having ordinary skill in the art at the time the invention was made to modify the devices of Applicant's Prior Art, Ono and Hioki by incorporating the transparent conductive film to comprise zinc oxide and indium oxide to prevent hillocks from being formed on first and second conductors as taught by Utsumi.

Allowable Subject Matter

Claims 62,64,68 and 70 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

Response to Arguments

Applicant's arguments filed 09 January 2007 have been fully considered but they are not persuasive. Applicant argues that the Applicant's Prior Art (Fig. 30) does not disclose both side surfaces of the connecting wiring in contact with the insulating film. This is erroneous as seen in Fig. 30, the side surface of the connecting wiring (3a) (the area on the left and right side of the connecting wiring) is connected to the insulating layer since layer 3a is directly contacting the insulating layer (3). Therefore the rejection stands.

Conclusion

THIS ACTION IS MADE FINAL. Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Kiesha L. Rose whose telephone number is 571-272-1844. The examiner can normally be reached on T-F 8:30-6:00 off Mondays.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Zandra Smith can be reached on 571-272-2429. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

KLR

March 30, 2007